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2 High-throughput, low-memory applications on the Pica architecture*Wills, D.S.; Cat, H.H.; Cruz-Rivera, J.; Lacy, W.S.; Baker, J.M., Jr.; Eble, J.C.; Lopez-Lagunas, A.; Hopper, M.;*

Parallel and Distributed Systems, IEEE Transactions on , Volume: 8 , Issue: 10 , Oct. 1997

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3 A high-speed shuffle bus for VLSI arrays*Lin, W.-T.; Hwang, J.-P.;*

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4 A new cryptographic system and its VLSI implementation*Jui-Cheng Yen; Hun-Chen Chen; Shin-Shian Jou;*

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5 Evaluation of Mobile Ethernet switch on network processor

Okubo, A.; Tsuzuki, M.; Hirano, Y.; Shimizu, K.; Kuroda, M.;

High Performance Switching and Routing, 2004. HPSR. 2004 Workshop on , 2
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